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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,865	08/21/2003	Hiroshi Komurasaki	009683-477	7048

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EXAMINER	
CHANG, JOSEPH	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/644,865	KOMURASAKI ET AL.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a spiral interconnection layer starting said first input/output terminal, and formed on a semiconductor substrate with an interlayer insulating film therebetween" in claims 2, 4, 7, 8, 12, 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Muramatsu et al. US Pub No. 2003/0146799 A1.

Regarding Claim 1, Muramatsu et al. discloses an oscillator circuit (Figures 2-6) for performing oscillation by positive feedback of an LC resonant circuit (inherent function in the structure of LC oscillator), wherein said LC resonant circuit (D1,D2,L1,L2, with switches SW1-4) includes a parallel resonant circuit formed of an inductance-variable portion (L1, L2, SW1-4) allowing variation of an inductance by a switch circuit (SW1-4) and a capacitor element (D1, D2) (Fig. 2 clearly shows the recited structure).

Regarding Claim 2. Muramatsu et al. discloses that the oscillator circuit (Fig 4-6) the inductance-variable portion (L1, L2, SW1-4) includes first (right side terminal of L1, 38) and second input/output terminals (end of 27 connecting current source 1), a spiral interconnection layer (38) starting from said first input/output terminal (right side terminal of L1, the end of 38), and formed on a semiconductor substrate (11) with an interlayer insulating film (26) therebetween, and a plurality of switch circuits (SW1, SW3) having

first terminals (ends of 38, 30 connecting SW1, SW3) connected to arbitrary positions on said interconnection layer (38 via 28, 30), and having second terminals (two center common nodes of SW1-4, 27) commonly connected to said second input/output terminal (end of 27 connecting current source 1), and when one of said plurality of switch circuits is turned on (SW1 is on), the position on said interconnection layer connected to said turned-on switch circuit is electrically coupled to said second input/output terminal (27 connects L1).

Regarding Claim 3, Muramatsu et al. discloses that the inductance-variable portion (L1, L2, SW1-4) further includes a plurality of second switch circuits (L2, SW2, SW4) each having a first terminal (right side of SW2) connected to the first terminal (ends of 38 connecting SW1) of one of said plurality of switch circuits (L1,SW1,SW3) (when SW1 is closed), and having a second terminal (right side of SW4) connected to the first terminal of another one of said plurality of switch circuits (end of 27 connecting current source 1) (It is noted that "connect" is a broad term that any two points are connected in any given circuit unless a modifier such as directly is recited), and when one of said plurality of switch circuits (SW1) and one of said plurality of second switch circuits (SW2) are turned on, the position on said interconnection layer connected to said turned-on switch circuit is electrically coupled to said second input/output terminal (end of 27 connecting current source 1).

Regarding Claim 4, Muramatsu et al. discloses that the plurality of switch circuits (SW1 and SW3) between trailing ends of the plurality of interconnection layers (see Fig. 4-6) and the second I/O terminal (27).

Regarding Claim 5. Muramatsu et al. discloses that the switch circuit includes a transistor element to be turned on/off in accordance with a voltage level of a control voltage (Para.[0050]).

Regarding Claim 6. Fig.2 shows capacitor element in said LC resonant circuit has a variable capacitance value (varactor diodes D1, D2).

Regarding Claim 7, Muramatsu et al. discloses in Fig.2, 4-6, an oscillator circuit, comprising: a pair of transistors cross-coupled to each other (Tr1 and Tr2); and an LC resonant circuit of a differential type (L1, L2, D1, D2) coupled to said pair of transistors in a feedback manner; wherein said LC resonant circuit includes first and second inductance-variable portions (L1, L2, D1, D2, SW1-4) including [first and second input/output terminals, said second input/output terminals being commonly connected to a fixed node, and said first and second inductance-variable portions being capable of varying inductances, and a first switch circuit coupled between the first input/output terminals of said first and second inductance-variable portions, each of said first and second inductance-variable portions has a spiral interconnection layer starting from said first input/output terminal and formed on a semiconductor substrate with an interlayer insulating film therebetween, and a plurality of second switch circuits having first terminals connected to arbitrary positions on said interconnection layer and second terminals commonly connected to said second input/output terminal, respectively, when one of said plurality of second switch circuits is turned on, the position on said interconnection layer connected to said turned-on second switch circuit is electrically coupled to said second input/output terminal, and when said first switch circuit is turned

on in response to the turn-on of said second switch circuit, said first switch circuit electrically couples said first and second inductance-variable portions.] (the limitations in [ ] are discussed in the Claims 1-6 rejections)

Regarding Claim 8, the scope of the claim is the same as the Claim 7 with trailing ends connections which Figures 4-6 show a plurality of second switch circuits coupled between trailing ends of said plurality of interconnection layers and said second input/output terminal, respectively, when one of said plurality of second switch circuits is turned on, the trailing end of said interconnection layer included in said plurality of interconnection layers and connected to said turned-on second switch circuit is electrically coupled to said second input/output terminal, and when said first switch circuit is turned on in response to the turn-on of said second switch circuit, said first switch circuit electrically couples said first and second inductance-variable portions.

Regarding Claim 9, Muramatsu et al. discloses that the first and second inductance-variable portions form a differential inductor element (Figure 2 shows a symmetrical structure which forms a differential inductor element).

Regarding Claim 10, Muramatsu et al. discloses that each of said first and second switch circuits includes a transistor element to be turned on/off in accordance with a voltage level of a control voltage (para.[0050]).

Regarding Claim 11, Muramatsu et al. discloses that the capacitor element in said LC resonant circuit has a variable capacitance value (varactors D1, D2).

Regarding Claims 12, 13, Muramatsu et al. discloses an L load differential circuit (Fig. 2, 4-6), comprising an inductor pair (L1, L2) including first and second

inductance-variable portions (SW1-4) having second input/output terminals (ends of 27) commonly connected to a fixed node (27) and being capable of varying inductances, and a first switch circuit coupled between first input/output terminals (left and right sides of L1 and L2) of said first and second inductance-variable portions, wherein each of said first and second inductance-variable portions has a plurality of spiral interconnection layers (38, 39). (See claims 1-6 rejections for repeating recitations).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

van Rumpt et al. discloses a VCO having a tunable parallel LC resonant circuit.

Washburn discloses an oscillator having a tapped inductor in the LC resonant circuit.

Eban discloses an oscillator having a tapped inductor in the LC resonant circuit.

Okamoto et al. discloses an LC oscillator having two spiral conductors on a semiconductor substrate.

Cruz et al. discloses a VCO having a variable inductor on a semiconductor substrate.

Shirai discloses a VCO having a LC oscillator with a controllable inductor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph Chang
Patent Examiner
Art Unit 2817